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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/941,478	08/29/2001	Jens Roever	US018133	6468
24738	7590	07/20/2006		
PHILIPS ELECTRONICS NORTH AMERICA CORPORATION INTELLECTUAL PROPERTY & STANDARDS 1109 MCKAY DRIVE, M/S-41SJ SAN JOSE, CA 95131				EXAMINER
				CHOI, WOO H
			ART UNIT	PAPER NUMBER
			2189	

DATE MAILED: 07/20/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>
	09/941,478	ROEVER, JENS
	<b>Examiner</b>	<b>Art Unit</b>
	Woo H. Choi	2189

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

1) Responsive to communication(s) filed on 01 June 2006.

2a) This action is FINAL.                            2b) This action is non-final.

3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

4) Claim(s) 9-16 is/are pending in the application.

4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.

5) Claim(s) \_\_\_\_\_ is/are allowed.

6) Claim(s) 9,10 and 13-15 is/are rejected.

7) Claim(s) 11,12,16 is/are objected to.

8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

9) The specification is objected to by the Examiner.

10) The drawing(s) filed on \_\_\_\_\_ is/are: a) accepted or b) objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) All    b) Some \* c) None of:

1. Certified copies of the priority documents have been received.
2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)	4) <input type="checkbox"/> Interview Summary (PTO-413)
2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)	Paper No(s)/Mail Date. _____ .
3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____ .	5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)
	6) <input type="checkbox"/> Other: _____ .

## **DETAILED ACTION**

### ***Claim Rejections - 35 USC § 102***

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 9, 10 and 13 – 15 are rejected under 35 U.S.C. 102(e) as being anticipated by Goeltzenleuchter *et al.* (US Patent No. 6,587,112, hereinafter “Goeltzenleuchter”).

3. With respect to claims 9 and 13, Goeltzenleuchter discloses a buffer management system for controlling access of a first buffer operation and a second buffer operation to a shared buffer (figure 2, 56) to prevent overwriting of data not yet read or reading of location to which valid data has not yet been written (col. 2, lines 19 – 39), comprising

a buffer manager that is configured to assert a wrap signal (figure 7, 104, means for indicating which buffer is the front buffer reads on this limitation) when a first buffer operation (write operation to the front buffer) involves consecutively accessing each buffer location of a block of buffer locations assigned sequential address values in an order different than an order defined by the sequential address values (figure 4, the buffer locations are accessed in an

interleaved manner), and is further configured to limit access to the buffer of a second buffer operation in dependence upon the wrap signal (read operation is limited to the front buffer).

4. With respect to claim 10, the first buffer operation includes an access that is based on a block address (figure 5A, 100K) and an offset address (offset-B, 400K), and the second buffer operation is limited to the block address when the wrap signal is asserted (read access is limited to the fill addresses of the back buffer), and is limited to a combination of the block address and the offset address when the wrap signal is deasserted (read operation uses the base address and offset of the appropriate buffer when the buffers are swapped again i.e., deasserting of the wrap signal).

5. With respect to claim 14, Goeltzenleuchter discloses a method of controlling access of a first buffer operation and a second buffer operation to a shared buffer to prevent overwriting of data not yet read or reading of locations to which valid data has not yet been written (see rejection of claim 9 above) comprising:

determining a block address (figure 5A, front buffer 100K) and an offset address (offset B, 72) corresponding to a first buffer operation involving consecutively accessing each buffer location of a block of buffer locations assigned sequential block address values,

determining when the offset address is non-sequential relative to the block address wherein the buffer locations are accessed in an order different than an order defined by the sequential address values (figure 4, fill command accesses the buffer locations in an interleaved manner), and

limiting a access of a second buffer operation (read cycle) to locations within the block when the offset address is non-sequential (figure 5B, offset C, read operation is limited to the back buffer of the 100X100 window, 78, that has a base address of 100K).

6. With respect to claim 15, the method further includes:

determining when the offset address is sequential relative to the block address (figure 5B, offset A), and limiting the second access to the buffer to a combination of the block address and the offset address when the offset address is sequential (figure 5B, read access is limited to the back buffer to a combination of a base or block address 100K and the offset address OFFSET A).

7. Claims 9 and 14 are rejected under 35 U.S.C. 102(e) as being anticipated by Chennubhotla *et al.* (US Patent No. 6,587,112, hereinafter “Chennubhotla”).

8. With respect to claims 9, Chennubhotla discloses a buffer management system (figures 1 and 2, col. 6, lines 53 – 62) for controlling access of a first buffer operation (first write operation) and a second buffer operation (a second write operation) to a shared buffer, to prevent overwriting of data not yet read or reading of locations to which valid data has not yet been written (buffer 200 may be a “circular buffer”, in a circular buffer read and write pointers that prevents overflow or underflow are implicit if not inherent as the would not operate properly without them), comprising:

a buffer manager that is configured to assert a wrap signal (write enable or equivalent signal that is inherent in a memory write operation) when the first buffer operation involves

consecutively accessing each buffer location of a block of buffer locations assigned sequential address values (col. 6, lines 44 – 52) in an order different than an order defined by the sequential address values (col. 6, lines 53 – 59), and is further configured to limit access to the buffer of a second buffer operation in dependence upon the wrap signal (when write enable signal is asserted, read access is not allowed).

9. With respect to claim 14, Chennubhotla discloses a method of controlling access of a first buffer operation and a second buffer operation to a shared buffer (figure 2, 200 and 2002, these are shared by multiple channels) to prevent overwriting of data not yet read or reading of locations to which valid data has not yet been written (see rejection of claim 9 above) comprising:

determining a block address (figure 5B, BASE32JBVM) and an offset address (offset indicated by DWORD#, groups or segments are accessed sequentially) corresponding to a first buffer operation involving consecutively accessing each buffer location of a block of buffer locations assigned sequential block address values (200 and 202 have sequentially addressed locations),

determining when the offset address is non-sequential relative to the block address wherein the buffer locations are accessed in an order different than an order defined by the sequential address values (access to 200 or 500 is non-sequential, col. 6, lines 53 – 67), and

limiting a access of the second buffer operation to locations within the block when the offset address is non-sequential (read or write access to the jitter buffer is always limited to the locations within the buffer).

***Allowable Subject Matter***

10. Claims 11, 12 and 16 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

***Conclusion***

11. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Woo H. Choi whose telephone number is (571) 272-4179. The examiner can normally be reached on M-F, 9:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Reginald Bragdon can be reached on (571) 272-4204. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Woo H. Choi  
July 18, 2006